REMARKS

Claims 1-33 are pending. In the Office Action dated March 29, 2006, the Examiner took the following action: (1) rejected claims 1-11, 13-17, 19-24 and 27-33 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Published Application No. 2005/0149603 to DeSota *et al.* ("DeSota") and in view of U.S. Published Application No. 2003/0156581 to Osborne ("Osborne"); (2) rejected claims 18 and 25 under 35 U.S.C. § 103(a) as being unpatentable over DeSota and Osborne as applied to claims 17 and 24 and in view of U.S. Published Application No. 2005/0015426 to Woodruff et al. ("Woodruff"); and (3) rejected claims 12 and 26 under 35 U.S.C. § 103(a) as being unpatentable over DeSota and Osborne as applied to claims 11 and 24 and in view of U.S. Patent No. 6,901,494 to Zumkehr et al. ("Zumkehr").

The disclosed examples of the invention will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed examples, and the discussion of the differences between the disclosed examples and the subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

The disclosed system is directed to a system and method for arbitrating memory responses in a hub-based memory system. The hub-based memory system includes a plurality of memory modules, each of which includes a memory hub coupled to a plurality of memory devices. The memory hub in each memory module serves basically two functions. First, it routes memory requests that are directed to memory devices on the same memory module to those memory devices. These memory requests are referred to as "local memory requests," and the responses to the local memory requests are referred to as "local memory responses." The memory hub also receives memory requests through the downstream link that are directed to memory devices on other, *i.e.* downstream, memory modules. These memory requests are referred to as "remote memory requests," and the memory hub passes these memory requests through a downstream link to the downstream memory module. The responses to the remote memory requests are referred to as "remote memory responses," and they are received by the

memory hub through an upstream link from the downstream memory module. The problem to which the disclosed system is directed is determining which memory responses the memory hub should output through the upstream link when both local memory responses and remote memory responses have been applied to the memory hub at the same time.

The disclosed system solves this problem by determining which memory response is triggered by the older memory request. The system performs this function by using a decoder to determine a memory request identifier associated with each memory request. This memory request identifier is then stored in a packet memory so that information about the order in which memory requests are received is available from a packet memory. As a result, it is possible to determine, based on the stored memory request identifiers, which memory request is older than another.

The disclosed system also includes a multiplexer that receives both the remote memory responses and the local memory responses. A control signal causes the multiplexer to couple to the upstream link either the remote memory responses or the local memory responses. This control signal is generated by arbitration control logic based on an examination of the memory request identifiers stored in the packet memory. More specifically, the arbitration control logic determines from the memory request identifiers stored in the packet memory the recentness of memory requests corresponding to the remote memory responses and the local memory responses. In this manner, the multiplexer can output the memory response to the oldest memory request.

It is important to recognize that the disclosed system and method is directed to solving a problem in a system in which a single device, *e.g.*, a memory hub controller, is accessing one of several other devices, *i.e.*, several memory modules. It is not directed to a system in which several devices are attempting to access a single device. That problem—arbitrating between several devices seeking access to a single device—is the function performed by the system disclosed in the DeSota *et al.* patent. Specificallly, the DeSota *et al.* system arbitrates between a first transaction directed to a resource of a first node, such as a memory device, and a second transaction from a second node that is also directed to the resource of the first node. In other words, two different nodes are attempting to engage in a transaction with the

same resource in the first node. In comparison to applicant's system, the DeSota *et al.* system is an entirely different type of arbitration system that performs an entirely different function.

Turning to the specific points in the Office Action, the Office Action asserts that the DeSota *et al.* patent discloses applicant's decoder as steps 102 and 104 in Figure 6. As explained above, applicant's decoder determines a memory request identifier associated with either local memory requests directed to memory devices on the same memory module or remote memory requests directed to memory devices in other modules. Step 102 in Figure 6 of the DeSoto *et al.* patent describes a situation in which a first node receives a transaction from a second node that relates to a resource of the first node. A typical node is shown in Figure 3. Thus, what is referred to in step 102 is a processor system receiving a transaction from another processor system for a resource, such as a memory 308, that is already being accessed by the first node processor system. Step 104 relates to determining that the first node is already being processed by the first node thereby requiring that the new transaction received from the second node be queued (Step 106'). These steps do not even remotely relate to the function of applicant's decoder of determining a memory request identifier associated with each memory request.

The Office Action also refers to the queues/registers 502, 506, 520 as corresponding to applicant's packet memory. However, these registers 502 and 506 store transactions that are directed to the same resource in the node containing the registers 502 and 506, which are coupled through the linked arbiter 512 to restart the transaction. Thus, while applicant's packet memory stores memory request identifiers that may be directed to several different resources, *e.g.*, several different local or remote memory devices, the registers 502 and 506 store transactions that are directed to the same resource.

As for the disclosed multiplexer, the Office Action does not even attempt to identify a corresponding structure disclosed in the DeSoto *et al.* patent. Instead, the Office Action merely refers to paragraphs 37-39 in Figure 8, which simply describes queuing a transaction directed to a resource in the first node that is already busy servicing an earlier transaction. Once processing of the earlier transaction has been completed, the new transaction is removed from the queue and is then processed. Applicant is at a loss to understand how this subject matter can possibly be considered to disclose a multiplexer selecting either remote

memory responses or local memory responses based on a control signal from an arbitrator, which examines the content of a packet memory that stores memory request identifiers.

In summary, the system described in the DeSota *et al.* patent is entirely different in both function and structure from applicant's disclosed system.

The patent to Osborne has been cited for disclosing a hub-based memory system. In applicant's disclosed memory hub system, each of a plurality of memory modules include a memory hub connected to a plurality of memory devices that are also contained in the memory module. While it is true that the memory system disclosed in Figure 1 does use a component 104 that is referred to as a memory controller hub, the memory controller hub 104 is simply a conventional system controller that couples memory requests from a CPU 108 to a memory device 110. The Osborne patent does not disclose a memory system in which a plurality of memory modules each contain a memory hub connected to a plurality of memory devices. Therefore, even if the teachings of the DeSota *et al.* patent were somehow combined with the teachings of the Osborne patent, the combined teachings would not result in a memory system having a plurality of memory modules, each of which include a memory hub and a plurality of memory devices coupled to the memory hub.

As the Examiner is undoubtedly aware, it is improper to combine the teachings of two or more prior references unless there is some suggestions in either reference of the desirability of combining their respective teachings. The Examiner has not even attempted to point out any portion of either the DeSota *et al.* patent or the Osborne patent that contains this necessary suggestion. Moreover, since the DeSota *et al.* patent describes a system for interfacing several nodes each of which comprise a computer system (*See*, Figure 3), and the Osborne patent describes a computer system, to the extent it would be obvious to combine the teachings of the references, the teachings would suggest using the Osborne computer system as the nodes in the DeSota *et al.* system. The result of this combination would not be a memory system that includes multiple memory module having respective memory hubs, each of which includes a multiplexer selecting either remote memory responses or local memory responses based on a control signal from an arbitrator, which examines the content of a packet memory that stores memory request identifiers.

Turning, now, to the claims, claim 1 is directed to a memory hub that includes a decoder. The decoder receives memory requests including local memory requests and remote memory requests. As explained above, the local memory requests are directed to memory devices connected directly to the memory hub on the same module, and the remote memory requests are directed to memory devices coupled to other memory hubs on other modules. The memory hub also includes a packet memory that is operable to receive and store the memory request identifiers from the decoder. A multiplexer, also included in the memory hub, couples either remote memory responses or local memory responses to an output control signal. As also explained above, the remote memory responses are received responsive to remote memory requests, and the local memory requests are received responsive to local memory requests. The control signal for the multiplexer is generated by arbitration control logic. The arbitration control logic accesses the packet memory and determines from the memory request identifiers stored in the packet memory the recency of the memory requests corresponding to the received remote memory responses and the local memory responses. The arbitration control logic then generates the control signal based on that determination. As explained above, the cited references, taking either alone or in combination, do not disclose or suggest a system having these components.

Claim 6 is directed to a memory hub that is operable to receive local memory responses and remote memory responses. The memory hub is operable to apply an arbitration algorithm to select the order in which the local and remote memory responses are provided on an uplink output based on the ages of the memory requests corresponding to the local and remote memory responses. As further explained above, none of the cited references, taken alone or in combination, suggest a system in which an arbitration algorithm is used to select either local or remote memory responses based on the ages of the corresponding memory requests.

Claim 11 is directed to a memory module containing the memory help of claim 1, and is therefore patentable for at least the same reasons that claim 1 is patentable. Similarly, claim 17 is directed to a memory system having a memory hub controller connected through a respective high-speed link to at least one memory module of the type recited in claim 11. Claim 17 is therefore patentable for at least the same reason that claim 11 is patentable. Finally, claim

24 is directed to a computer system including the memory modules of the type recited in claim 11, and is therefore also patentable over the cited references.

The final independent claim is claim 29, which is directed to a method of processing and forwarding memory responses in the memory hub of a memory module that is part of a memory system. The method includes receiving memory requests, including local memory requests and remote memory requests. The memory requests each include a memory request identifier, which are stored in the memory hub. Local memory responses and remote memory responses are also stored. The claim also requires that at least one arbitration algorithm is applied in the hub based on the ages of the stored memory request identifiers to determine in which order the stored local and remote memory responses are forwarded upstream. Clearly, none of the cited references, taken alone or in combination, suggest these steps, as explained in detail above.

The remaining claims, which are dependent on the above-discussed independent claims, patentably distinguish over the cited references because of their dependency on patentable independent claims and because of the additional limitations added by those claims.

All of the claims in the application are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,
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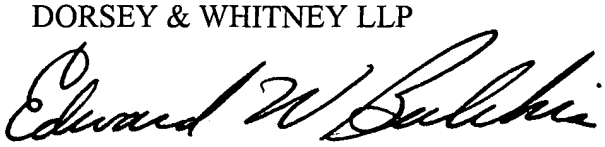

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